Claim Amendments

Please amend claims 1, 6, 14, and 16 as follows:

Listing of Claims

1. (currently amended) A method for improving a polysilicon gate electrode profile to avoid preferential RIE etching in a polysilicon gate electrode etching process comprising the steps of:

providing a semiconductor process wafer comprising a gate dielectric formed over a silicon substrate and a polysilicon layer formed over the gate dielectric;

providing a hardmask layer over the polysilicon layer;

carrying out a first reactive ion etch (RIE) step to etch through a thickness of the hardmask layer to expose the polysilicon layer to form a patterned hard mask for forming a gate electrode;

carrying out a second RIE step to etch through a first thickness portion of the polysilicon layer including an RF source power and an RF bias power;

carrying out a third RIE step to etch through a second

thickness portion of the polysilicon layer to endpoint detection to expose portions of an underlying gate dielectric including using lower etch power compared to the second RIE step, said lower power selected from the group consisting of a lower RF source power and a lower RF bias power; and,

then plasma treating the exposed gate dielectric and polysilicon layer in-situ ~~wherein the plasma is formed essentially from an inert source gas~~ with an inert gas plasma to neutralize an electrical charge imbalance.

2. (original) The method of claim 1, wherein the step of plasma treating is carried out using zero RF bias power.

3. (previously presented) The method of claim 1, further comprising an RIE overetch step carried out using zero RF bias power.

4. (original) The method of claim 1, wherein the polysilicon layer includes an n-dope region and a p-doped region for forming respectively doped polysilicon gate electrodes in parallel.

5. (original) The method of claim 1, wherein the RF source power

and RF bias power are reduced in the third RIE Step.

6. (currently amended) The method of claim 1, wherein the inert gas ~~source~~ is selected from the group consisting of argon, helium, nitrogen, and mixtures thereof.

7. (previously presented) The method of claim 1, further comprising an RIE overetch step carried out with a chlorine-free etching chemistry.

8. (original) The method of claim 7, wherein the chlorine-free etching chemistry comprises HBr and oxygen.

9. (previously presented) The method of claim 1, wherein the second and third RIE etch steps have an etching chemistry comprising constituents selected from the group consisting of $HBr/Cl_2/O_2$ and $CF_4/Cl_2/O_2$.

10. (original) The method of claim 1, wherein the RF bias power is supplied at a frequency of greater than about 1 MHz adjustably decoupled from the RF source power.

11. (original) The method of claim 1, wherein the gate dielectric

is selected from the group consisting of thermally grown SiO_2 and binary oxides having a dielectric constant of greater than about 20.

12. (original) The method of claim 1, wherein the hardmask layer is selected from the group consisting of silicon oxide, silicon nitride, and silicon oxynitride.

13. (original) The method of claim 1, wherein the third RIE etch step is carried out with zero RF bias power applied.

14. (currently amended) A method for improving a polysilicon gate electrode profile to avoid preferential RIE etching in parallel etching of n and p-doped polysilicon gate electrodes comprising the steps of:

providing a semiconductor process wafer comprising a gate dielectric formed over a silicon substrate and a polysilicon layer including n-doped and p-doped regions formed over the gate dielectric;

providing a hardmask layer over the polysilicon layer;

carrying out a first reaction ion etch (RIE) step to etch through a thickness of the hardmask layer to expose portions of the polysilicon layer to thereby form a patterned hard mask for forming gate electrode;

carrying out a second RIE step to etch through a first thickness portion of the polysilicon layer including an RF source power and an RF bias power.

carrying out a third RIE step to etch through a second thickness portion of the polysilicon layer to endpoint detection to expose portions of an underlying gate dielectric using lower etch power compared to the second RIE step, said lower power selected from the group consisting of a lower RF source power and a lower RF bias power;

then plasma treating in-situ with an inert gas plasma the exposed gate dielectric and polysilicon layer using a zero RF bias power to neutralize an electrical charge imbalance; and,

then carrying out an RIE overetch process to remove a remaining portion[[s]] of the polysilicon layer using a zero RF bias power.

15. (original) The method of claim 14, wherein the RF source power and RF bias power are reduced in the third RIE Step.

16. (currently amended) The method of claim 14, wherein the inert gas ~~source~~ is selected from the group consisting of argon, helium, nitrogen, and mixtures thereof.

17. (previously presented) The method of claim 14, wherein the RIE overetch is carried out with a chlorine-free etching chemistry.

18. (original) The method of claim 17, wherein the chlorine-free etching chemistry comprises HBr and oxygen.

19. (previously presented) The method of claim 14, wherein the second and third RIE etch steps have an etching chemistry selected from the group consisting of HBr, Cl_2, CF_4, and O_2.

20. (original) The method of claim 14, wherein the RF bias power is supplied at a frequency of greater than about 1 MHz adjustably decoupled from the RF source power.

21. (original) The method of claim 14, wherein the gate dielectric is selected from the group consisting of thermally grown SiO_2 and binary lanthanum oxides having a dielectric constant of greater than about 20.

22. (original) The method of claim 14, wherein the hardmask layer is selected from the group consisting of silicon oxide, silicon nitride, and silicon oxynitride.

23. (previously presented) The method of claim 14, wherein the third RIE etch step is carried out with zero RF bias power applied.